CLAIMS

What is claimed is:

1. A data-retention circuitry comprising:

data-retention subcircuits in a feedback loop; and

a supply-switching subcircuit to provide current to the data-retention subcircuits from a supplemental voltage supply through a well tap during a standby mode.

2. The data-retention circuitry of claim 1 further comprising an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal,

wherein the supply-switching subcircuit is to switch from a regular voltage supply to the supplemental voltage supply in response to the sleep signal, and

wherein the isolation subcircuit is to pass data signals between the data-retention subcircuits and the pass-gate subcircuit when voltage from the regular voltage supply is present.

3. The data-retention circuitry of claim 1 wherein the data-retention subcircuits are to retain a state when receiving current from the supplemental voltage supply.

4. The data-retention circuitry of claim 2 wherein the pass-gate subcircuit is to pass a latched state signal to the isolation subcircuit in response to a clock signal.

5. The data-retention circuitry of claim 2 wherein the data-retention subcircuits, the switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices.

6. The data-retention circuitry of claim 2 wherein the data-retention subcircuits are coupled in series in the feedback loop, and wherein the data-retention circuitry comprises an output inverter to receive a state signal from one of either the isolation subcircuit or the pass-gate subcircuit and to provide an output signal.

7. The data-retention circuitry of claim 1 wherein the supply-switching subcircuit comprises a semiconductor switching subcircuit that is part of a semiconductor die, the semiconductor die having a well-tap to provide the current from the supplemental voltage supply, and

wherein the semiconductor switching subcircuit is to couple the data-retention subcircuits to the regular voltage supply when the semiconductor switching subcircuit receives a first state of the sleep signal, and wherein current is to flow to the data-retention subcircuits from the well-tap when the semiconductor switching subcircuit receives a second state of the sleep signal.

8. The data-retention circuitry of claim 2 wherein the regular and supplemental voltage supplies are provided by a single voltage source, the regular voltage supply being decoupled from the supplemental voltage supply during the standby mode.

9. The data-retention circuitry of claim 2 further comprising a master latch to latch a state signal, and wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch, and

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to a clock signal.

10. The data-retention circuitry of claim 9 wherein circuits of the master latch are to receive power from the regular voltage supply, and wherein during the standby mode the regular voltage supply is turned off.

11. The data-retention circuitry of claim 9 wherein the data-retention subcircuits, switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and wherein the pass-gate subcircuit and master latch comprise higher-leakage semiconductor devices, the lower-leakage devices having at least one of either a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

12. A processing system comprising:

a processor on a semiconductor die; and

a data-retention circuitry on the semiconductor die to retain state information for the processor during a standby mode, wherein the data-retention circuitry comprise data-retention subcircuits to receive current through a well tap in the semiconductor die during the standby mode to retain the state information.

13. The system of claim 12 wherein the data-retention circuitry further comprise an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to provide current to the data-retention subcircuits from a supplemental voltage supply through the well tap during the standby mode.

14. The system of claim 12 wherein the data-retention circuitry are arranged in cells on the semiconductor die, the cells having at least one well tap to provide the current from the supplemental voltage supply of an associated one of the cells.

15. The system of claim 13 wherein the supply-switching subcircuit is to switch from a regular voltage supply to the supplemental voltage supply in response to a sleep signal, and

wherein the isolation subcircuit is to pass data signals between the data-retention subcircuits and the pass-gate subcircuit when voltage from the regular voltage supply is provided.

16. The system of claim 13 wherein the pass-gate subcircuit is to pass a latched state signal to the isolation subcircuit in response to a clock signal.

17. The system of claim 16 wherein the data-retention circuitry further comprise a master latch to latch a state signal, and

wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch, and

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to a clock signal.

18. The system of claim 17 wherein circuits of the master latch are to receive current from the regular voltage supply, and wherein during the standby mode the regular voltage supply is turned off.

19. The system of claim 17 wherein the data-retention subcircuits, switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and wherein the pass-gate subcircuit and the master latch comprise higher-leakage semiconductor devices, the lower-leakage devices having at least one of either a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

20. A method comprising:

isolating data-retention subcircuits in response to a sleep signal;

switching the data-retention subcircuits to receive current from a supplemental voltage supply in response to the sleep signal; and

retaining state information by the data-retention subcircuits when receiving the current from the supplemental voltage supply during a standby mode.

21. The method of claim 20 further comprising providing the current from the supplemental voltage supply through a well-tap on a semiconductor die.

22. The method of claim 20 wherein switching further comprises switching from a regular voltage supply to the supplemental voltage supply in response to the sleep signal.

23. The method of claim 22 further comprising passing state information between the data-retention subcircuits and a pass-gate subcircuit when the regular voltage supply is present at an isolation subcircuit.

24. A wireless communication device comprising:

an omnidirectional antenna to communicate radio-frequency signals;

a processor on a semiconductor die to convert between the radio-frequency signals and data signals; and

a data-retention circuitry on the semiconductor die to retain state information for the processor during a standby mode, wherein the data-retention circuitry comprise data-retention subcircuits to receive current through a well tap in the semiconductor die during the standby mode to retain the state information.

25. The device of claim 24 wherein the data-retention circuitry further comprise an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to provide current to the data-retention subcircuits from a supplemental voltage supply through a well tap during the standby mode.

26. The device of claim 25 wherein the data-retention subcircuits, switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and wherein the pass-gate subcircuit comprises higher-leakage semiconductor devices, the lower-leakage devices having at least one of either a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.